UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,032	03/26/2004	Alexander Levin	42P18580	9556

8791 7590 02/21/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,032	LEVIN, ALEXANDER	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-4, 11, 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Rokhsaz (6,566,950)

Claim 1, Rokhsaz shows a predriver circuit for a differential output driver comprising:

a pull-up circuit (82, 86, Fig. 3) having at least one pull-up device of a first device type (NMOS); and a pull-down circuit (84, 88) including at least one pull-down device of the first device type (NMOS) having a source coupled to ground (the source of 84 and 88 are coupled to ground), the pull-up circuit and the pull-down circuit to charge an output node and a complement output node in opposite directions to generate a low swing differential predriver signal pair to open/close a pair of line driver switches (36, 38) of the output driver of a second device tvpe (PMOS) to generate a differential output driver signal pair for a pair of output pads (differential output 24) coupled to the pair of line driver switches to provide the differential output driver signal pair onto a

motherboard (circuit board, col. 3, lines 43-50) for communication over a serial interconnect.

Claim 3, Rokhsaz shows the predriver circuit of claim 1, wherein the pull-up device and the pull-down device comprise NMOS devices (82 and 86 are NMOS) and wherein the pair of line driver switches comprise PMOS devices (36 and 38 are PMOS).

Claim 4, Rokhsaz shows the predriver circuit of claim 1, wherein the pull-up circuit comprises: a first pull-up device (82) having a gate coupled to a data input signal (22) , a drain coupled to a power supply (VDD) and a source coupled to the output node (to gate 40 and 38); and a second pull-up device (86) having a gate coupled to a complement input signal (22 which differential signal), a drain coupled to the power supply (VDD) and a source coupled to the complement output node (output to gates 42 and 36).

Claim 11, Rokhsaz shows a predriver circuit including:

An output driver circuit, comprising: a pull-up circuit (82 and 86, Fig. 3) having at least one pull-up device of a first device type (NMOS), and a pull-down circuit (84 and 88) including at least one pull-down device of the first device type (NMOS) having a source coupled to ground, the pull-up circuit and the pull-down circuit to charge an output node (output to gates 40 and 38) and a complement output node (output to gates 42 and 36) in opposite directions to generate a differential predriver signal pair, including a predriver signal and a complement predriver signal (the signal is differential indicated as differential input amplifier 30);

and a line driver (30 and 32) including:

a first switch (38) of a second device type (PMOS) to generate a complement output driver signal in response to the predriver signals a second switch (36) of the second device type to generate an output driver signal in response to the complement predriver signal,

a first output pad (output 24 coupled through transistor 70) coupled to the first switch to provide the complement output driver signal onto a motherboard (circuit board, col. 3, lines 43-50) for communication over a serial interconnect and a second output pad (output 24 coupled through transistor 68) coupled to the second switch to provide the output driver signal onto the motherboard for communication over the serial interconnect.

Claim 13, Rokhsaz shows the output driver circuit of claim 11, wherein the pull-up device and the pull-down device comprise NMOS devices (82, 84, 86, 88 are PMOS) and wherein the first and second switches comprises PMOS devices (36, 38, 40, 42 are PMOS).

Claim 14, Rokhsaz shows the predriver circuit of claim 1, wherein the pull-up circuit comprises: a first pull-up device (82) having a gate coupled to a data input signal (22) , a drain coupled to a power supply (VDD) and a source coupled to the output node (to gate 40 and 38); and a second pull-up device (86) having a gate coupled to a complement input signal (22 which differential signal), a drain coupled to the power supply (VDD) and a source coupled to the complement output node (output to gates 42 and 36).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Khoury et al. (5,959,492).

Khoury shows an electronic system comprising:

a motherboard (printed circuit board, col. 8, lines 34-35) on which a serial interconnect is formed, an integrated circuit (IC) chip package (packaged integrated circuit, col. 8, lines 34-35) being operatively installed on the board to communicate using the serial bus, the package having an IC chip (inherent limitation since an IC chip in the package include core circuit and an I/O section for outputting the signals) that includes a logic function section and an I/0 section as an interface between the logic function section and the serial bus, the I/0 section having an output driver (Fig. 4A) in which a pre-driver (402) includes a pull-up circuit (115, 126, 124, 123) having at least one pull-up device of a first device type (PMOS), and a pull-down circuit (116 and 114) having at least one pull-down device of the first device type (PMOS), the pull-up circuit and the pull-down circuit to charge an output node and a complement output node in opposite directions to generate a differential predriver signal pair (120 and 122) to open/close a pair of line driver switches (128 and 130) to generate a differential output driver signal pair for a pair of output pads (160a and 162a) coupled to the pair of line driver switches to provide the differential output driver signal pair onto the motherboard (printed circuit board) for communication over the serial interconnect, wherein the pull-up device is cross-coupled to the pull-down devices (115 and 114 is cross-coupled) and

wherein the pair of line driver switches are of a second device type (128 and 130 are NMOS).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 9-15, 19-20, 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dally et al. (6,965,299) in view of Rokhsaz (6,566,950).

Claim 1, Dally shows a predriver circuit (110, Fig. 3 and 7) for a differential output driver comprising:

a pull-up circuit (111 and 114, Fig. 3) having at least one pull-up device of a first device type (NMOS); and a pull-down circuit (113 and 112) including at least one pull-down device of the first device type (NMOS) having a source coupled to ground (the source of 112 and 113 are coupled to ground), the pull-up circuit and the pull-down circuit to charge an output node and a complement output node in opposite directions to generate a low swing differential predriver signal pair to open/close a pair of line driver switches (137 and 138, Fig. 9 that is in 160, Fig. 7) of the output driver of a second device tvpe (PMOS) to generate a differential output driver signal pair for a pair of output pads (yP and yN) coupled to the pair of line driver switches to provide the differential output driver signal.

Dally discloses the claimed invention except for an output communication lines are on a motherboard.

However, Rokhsaz discloses an output communication lines may incorporated on a printed circuit board (motherboard) along with another electronic device (col. 3, lines 43-50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit (Fig. 7) of Dally on a printed circuit board, in order to transmit or transport communication signals to another electronic device.

Claim 2, Dally in view of Rokhsaz shows the predriver circuit of claim 1, wherein the pull-up device is cross-coupled to the pull-down device (111 and 114 are cross-coupled).

Claim 3, Dally in view of Rokhsaz shows the predriver circuit of claim 1, wherein the pull-up device and the pull-down device comprise NMOS devices (they are NMOS) and wherein the pair of line driver switches comprise PMOS devices (137 and 138 are PMOS).

Claim 4, Dally in view of Rokhsaz shows the predriver circuit of claim 1, wherein the pull-up circuit comprises: a first pull-up device (11) having a gate coupled to a data input signal (dP), a drain coupled to a power supply (VDD) and a source coupled to the output node (xP); and a second pull-up device (114) having a gate coupled to a complement input signal (dN), a drain coupled to the power supply (VDD) and a source coupled to the complement output node (xN).

Claim 5, Dally in view of Rokhsaz shows the predriver circuit of claim 1, wherein the pull-down circuit comprises: a first pull-down device (113) having a gate coupled to a complement input signal, a drain coupled to the output node and a source coupled to ground; and a second pull-down device (112) having a gate coupled to a data input signal, a drain coupled to the complement output node and a source coupled to ground.

Claim 9, Dally in view of Rokhsaz shows the predriver circuit of claim 2, further comprising:

a first pull-up device (111) cross-coupled to a first pull-down device (112) to receive a data input signal (dP) and to charge the output node and the complement output node in opposite directions;

a second pull-up device (114) cross-coupled to a second pull-down device (113) to receive a complement data input signal and to charge the output node and the complement output node in opposite directions to generate the differential predriver signal pair.

Claim 10, Dally in view of Rokhsaz shows the predriver circuit of claim 9, wherein the first and second pull-up devices comprise NMOS devices and the first and second pull-down devices comprise NMOS devices (they are all NMOS).

Claim 11, Dally shows a predriver circuit including:

An output driver circuit, comprising: a pull-up circuit (111 and 114, Fig. 3) having at least one pull-up device of a first device type (NMOS), and a pull-down circuit (113 and 112) including at least one pull-down device of the first device type (NMOS) having a source coupled to ground, the pull-up circuit and the pull-down circuit to charge an

output node (xP) and a complement output node (xN) in opposite directions to generate a differential predriver signal pair, including a predriver signal and a complement predriver signal;

and a line driver (160, Fig. 7 shown in Fig. 9) including:

a first switch (137) of a second device type (PMOS) to generate a complement output driver signal in response to the predriver signals a second switch (138) of the second device type to generate an output driver signal in response to the complement predriver signal,

a first output pad (yP which coupled through 110, Fig. 9) coupled to the first switch to provide the complement output driver signal for communication over a serial interconnect and a second output pad (yN which coupled through 110, Fig. 9) coupled to the second switch to provide the output driver signal for communication over the serial interconnect.

Dally discloses the claimed invention except for an output communication lines are on a motherboard.

However, Rokhsaz discloses an output communication lines may incorporated on a printed circuit board (motherboard) along with another electronic device (col. 3, lines 43-50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit (Fig. 7) of Dally on a printed circuit board, in order to transmit or transport communication signals to another electronic device.

Claims 12-15, 19, 20, and 26-30, the limitations of the claims are rejected as above claims 1-5, 9 and 10.

6. Claims 6-8 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dally et al. (6,965,299) in view of Rokhsaz (6,566,950) and further view of Bass (6,407,590).

Dally in view of Rokhsaz discloses the claimed invention except for a first NMOS transistor having a gate and a drain connected to the output node and a source coupled to ground, a second NMOS transistor having a gate and a drain connected to the complement output node and a source coupled to ground.

Bass shows a first NMOS transistor (30, Fig. 1) having a gate and a drain connected to the output node (40) and a source coupled to ground (VSS), a second NMOS transistor (32) having a gate and a drain connected to the complement output node (38) and a source coupled to ground.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the output node and the complement output node of Dally with a first NMOS transistor having a gate and a drain connected to the output node and a source coupled to ground, a second NMOS transistor having a gate and a drain connected to the complement output node and a source coupled to ground as Bass, in order to clamp the differential output swing from becoming too large.

7. Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury et al. (5,959,492).

Khoury discloses the claimed invention except for the logic function section is microprocessor, a memory controller, a bus bridge, or an I/O controller. It would have been an obvious matter of design choice to provide the logic function section as a microprocessor, a memory controller, a bus bridge, or an I/O controller, since applicant has not disclosed that the logic function section is microprocessor, a memory controller, a bus bridge, or an I/O controller solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the logic function section is microprocessor, a memory controller, a bus bridge, or an I/O controller.

8. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khoury et al. (5,959,492) in view of Martin et al. (6,894,536).

Khoury shows an output differential driver including: a predriver circuit (402, Fig. 4A) comprising:

a pull-up circuit (115, 126, 124, and 123) having at least one pull-up device of a first device type (PMOS), a pull-down circuit (116, 114 and NMOS connected between node 118 and VSS) including at least one pull-down device of the first device type having a source coupled to ground (VSS), the pull-up circuit and the pull- down circuit to charge an output node and a complement output node in opposite directions to generate a differential predriver signal pair (120 and 122) including a predriver signal and a complement predriver signal, and a line driver comprising: a first switch of a

second device type (128 is an NMOS) to generate a complement output driver signal in response to the predriver signal, a second switch (130) of the second device type to generate an output driver signal in response to the complement predriver signal, a first output pad (160a) coupled to the first switch to provide the complement output driver signal, and a second output pad (162a) coupled to the second switch to provide the output predriver signal.

Khoury discloses the claimed invention except for a chipset coupled to a processor via a serial interconnect and the chipset include a differential driver.

Martin discloses a chipset (62, Fig. 5) coupled to a processor (60) via a serial interconnect (14) and the chipset include a differential driver (16 which is a differential I/O port).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the output differential driver of Khoury in a chipset coupled to a processor by a serial interconnect, in order to provide interconnects between functional units within a computer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

2/16/06